Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L15	L3 and l5	3	L15
L14	L5 same compress	1	L14
L13	L4 same l3	17	L13
L12	L11 same l7	16	L12
L11	L4 same circuit	1193	L11
L10	L9 same l8	2	L10
L9	external near3 command	6637	L9
L8	L7 same storage	3202	L8
L7	address adj1 generat$	18014	L7
L6	L5 same l3	0	L6
L5	L4 adj1 circuit	198	L5
L4	scrambling	5475	L4
L3	L2 same l1	8239	L3
L2	(ad or a/d) adj1 converter	49860	L2
L1	processor	240590	L1

END OF SEARCH HISTORY

WEST

End of Result Set

Generate Collection Print

L15: Entry 3 of 3 File: USPT Jul 14, 1987

DOCUMENT-IDENTIFIER: US 4680791 A
TITLE: Digital video signal process apparatus for use in a video tape recorder

Drawing Description Text (3):
FIG. 2(a) is a block diagram showing a construction of the scrambling circuit and a descrambling circuit of FIG. 1;

Detailed Description Text (2):
The invention will now be described in detail with reference to the accompanying drawings. FIG. 1 is a block diagram of a PCM-VTR wherein the present invention is applied. The apparatus includes, in series, a record processor 1, a modulator 2, a magnetic head 3, a magnetic tape 4, a demodulator 5, a time base corrector 6 and a reproducing processor 7. The record processor 1 comprises an A/D converter 8, a time base compresser 9, a parity generator 10, a scrambler 11, and a SYNC generator 12. The modulator 2 comprises an encoder 13 and a recording amplifier 14. The magnetic head 3 comprises a recording head 15 and a reproducing head 16. The demodulator 5 comprises a reproducing amplifier 17 and a decoder 18. The reproducing processor 7 comprises a descrambler 19, an error correction/concealment circuit 20, a time base expander 21, and a D/A converter 22.

Detailed Description Text (4):
Returning to FIG. 1, input video signal 40 is converted into a digital signal by the A/D converter 8 (FIG. 1), and the digital signal is transformed into a recording signal 42 having a recording format as shown in FIG. 3 by the time base compresser 9. The recording format is constructed as follows. Effective video data of 768 bits (when a sampling frequency of four times subcarrier frequency is used) from one horizontal period (H) is divided into eight equal parts. A synchronizing code (SYNC) of 40 bits and a CRC code of 16 bits are added to each divided part so as to make up a sub-block (SB). A correction code of 8 sub-blocks is then added to each data group of 64 sub-blocks so as to make up a block (B). As a result, one vertical period (V) is composed of 32 blocks. To this end, a signal delivered from the time base compressor 9 is supplied to the parity generator 10 which adds the correction code and CRC code. The output of the parity generator is then supplied to the scrambling circuit 11.

Detailed Description Text (5):
As shown in FIG. 2a, the scrambling circuit 11 can be assembled in a serial byte configuration. The matrix calculator 24 delivers a pseudo-random signal which is obtained by dividing the address signal ADSY sequentially by a generator polynomial G(X)=X.sup.8 +X.sup.6 +X.sup.5 +X.sup.4 +1. In this case, the pseudo-random signal corresponds to a remainder in the aforementioned dividing calculation. The pseudo-random signal is supplied to the register 25 with register 25 being reset by a timing signal Ts which is synchronized with the sub-block. Accordingly, in the pseudo-random signal from the register 25, synchronism is obtainable at each timing signal Ts (sub-block timing). Furthermore, since the address signal ADSY varies according to 72 sub-blocks as shown in FIG. 4 (c), a pseudo-random signal varying in its content at every sub-block is generated. A scrambled signal is then obtained by adding the pseudo-random signal to the input signal in a manner of MOD2 in the exclusive OR circuit 26. The synchronization code (SYNC) shown in FIG. 4 (a) is added to the scrambled signal in the SYNC generator 12 (FIG. 1). As shown in FIGS. 4 (a), 4 (b) and 4 (c), the SYNC signal comprises 5 bytes (40 bits), which includes 4 bytes of address data (SY0 to SY3) all common and 1 byte of the address signal ADSY varying in its content at every sub-block SB. The output 44 of the SYNC generator 12 is converted into the recording signal 46 by the encoder 13, and the recording signal 46 is supplied through the recording amplifier 14 to the recording head 15.

CLAIMS:

8. A scrambling circuit for encoding a video signal, said video signal being of the type which is divided into a plurality of blocks, each block being further subdivided into a plurality of sub-blocks, each sub-block having a plurality of fields including a sync field, a data field and an error correction field, said circuit comprising:

means for generating and appending to each one of said sub-blocks a unique address field for identifying said sub-block;

a pseudo-random source for supplying a sequence of pseudo-random values;

means for modulating the pseudo-random values with the address information associated with said sub-blocks, and for generating a pseudo-random signal comprised of said sequence of said pseudo-random values modulated by said address information; and

means for scrambling at least said data field with said pseudo-random signal.

12. The circuit of claim 11, further comprising means for deriving from said scrambled video signal a clock signal for synchronizing said scrambling circuit and said decoding means to one another.

WEST

End of Result Set

Generate Collection Print

L14: Entry 1 of 1 File: USPT Mar 7, 2000

DOCUMENT-IDENTIFIER: US 6035044 A
TITLE: Scrambling type method and apparatus for video transmission/receipt

Brief Summary Text (21):
In addition, in accordance with the present invention, a video transmitter/receiver includes a main scrambling circuit for executing main soft scrambling with an original video signal to thereby output a main scrambled signal. A compressing circuit compresses the main scrambled signal to thereby output a compressed video signal. An auxiliary scrambling circuit executes auxiliary soft scrambling with the compressed video signal to thereby output an auxiliary scrambled signal. The auxiliary scrambled signal is sent as a signal to be transmitted

WEST

Generate Collection Print

L15: Entry 2 of 3 File: USPT Dec 20, 1994

DOCUMENT-IDENTIFIER: US 5374952 A
** See image for Certificate of Correction **
TITLE: Videoconferencing system

Detailed Description Text (24):
Conversely, the video signal received from the camera unit 11 is passed through a video signal control 88 (FIG. 5B) to an RF modulator 80. The audio signal received from a microphone in the camera unit is also passed through the audio signal control to the RF modulator 80. This audio signal may be sampled and digitized in an A/D converter in an audio processor 92 and then supplied to the PC for storage on a hard disk for subsequent retrieval and "playback". The retrieved digital signal is passed to a D/A converter in the processor 92 and then transmitted via the audio signal control 86 to the speaker or handset, or to the audio input of the modulator 80.

Detailed Description Text (88):
The circuit of FIG. 24A may be inserted in the video signal stream to "scramble" the video signal prior to RF modulation. This circuit comprises a sync extractor 230 which passes timing signals to a microprocessor 232. The microprocessor generates control signals which are passed to a scrambling circuit 234. The scrambling circuit adds (or subtracts) a different DC voltage to each successive scan line, inverts the signal of every other scan line, or effects some other simple change that causes the image to "disappear" if displayed without descrambling.

Detailed Description Text (89):
FIG. 24B illustrates how the scrambled video signal is descrambled. A sync extractor 236 provides timing signals to a microprocessor 238 which, in turn, generates control signals for the descrambling circuit 240. The descrambling circuit effectively removes whatever change was made to the signal, scan line by scan line, by the scrambling circuit 234.

WEST

Generate Collection Print

L10: Entry 1 of 2 File: USPT Aug 7, 2001

DOCUMENT-IDENTIFIER: US 6272084 B1
** See image for Certificate of Correction **
TITLE: Memory controller, reproducing apparatus mounting the same and method for controlling the same

Brief Summary Text (34):
The foregoing object and other objects of the invention have been achieved by the provision of a disc reproducing apparatus having a recording medium 3 in which the data composed of, at least, sync data, header data, and digital data is recorded, and a storage means 10 which sequentially reads from the data of sector unit from a recording medium 3 and which once storages the data, in which the data stored in the storage means 10 is sequentially read for every sector unit and is reproduced, comprises: a recording control means 8 for controlling the write/read of said digital data to said recording means; and a control means 9 for controlling the operation state of said recording control means 8, wherein: said recording control means 8 has address generating parts 27 and 28 for generating an internal address of said storage means 10 according to the external command (R/W control signal) transferred from said control means 9 and/or the data (status) read to said storage means 10. Further, in the present invention, said control means 9 switches to one of the round mode that the internal address of said storage means 10 generated by the address generating part 27 specify the address in the same area repeatedly, the straight mode for specifying the address in the next area after the specification of the address in one area terminates, and the re-try mode for specifying the address in the front area after the specification of address in one area terminates.

Brief Summary Text (37):
Address generating parts 27 and 28, which generate the internal address of a storage means 10 according to the external command (R/W control signal) outputted from a control means 9 and/or the data (status) read into the storage means 10 are provided to the store control means 8 controlling the write/read of the digital data to the storage means 10. The address generating parts 27 and 28 control the write/read of the data to the storage means 10 based on the generated address. This simplifies the specification of address, and complicated control becomes needless.

Brief Summary Text (38):
According to this invention, an address generating part is provided in a storage control means for controlling the write/read of the digital data to a storage means, in order that the internal address in the storage means is generated according to the external command transferred from a control means and/or the data read to the storage means. Therefore, the necessary confirmation for writing the data becomes once for each sector, and this simplifies the specification of address in comparison with the conventional processing so as to reduce a load of the control circuit.